Amendments to the Specification:

Please replace paragraph 1, page 11 with the following amended paragraph:

In this manner, if any two (or more) hit signals indicate a hit, two series-coupled pull-down transistors will be turned on and output node 212 of Figure 2 will be pulled down. Voltage clamp 211 includes an inverter having an input coupled to output node 212 of the NAND and having an output that provides the error flag. Thus, if any two hit signals indicate a hit, the error flag will go high, indicating the presence of a multi-hit error and further indicating that the selected data from the cache is invalid and should not be used.

Please replace paragraph 1, page 12 with the following amended paragraph:

At step 305 of Figure 3, data is selected from the appropriate memory location of the cache based on the hit signals. This may be accomplished by a multiplexer having select inputs coupled to the hit lines to receive the hit signals as described above. In accordance with one embodiment of the present invention, step 305 occurs simultaneously with steps 310, 315, 320 and 325. As used herein, the term "simultaneously" means that the time it takes for a first event to occur overlaps with the time it takes for a second event to occur. The first and second events need not begin and end at the same time to be considered simultaneous.